A 44 GHz InP-based HBT Double-Balanced Amplifier with Novel Current Re-use Biasing

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Abstract

Here we report on what is believed to be the first Q-band IP3 results of an InAlAs/InGaAs-InP based HBT MMIC linear amplifier. The 3-stage amplifier uniquely combines a "double-balanced" design topology that incorporates a "current re-use" bias scheme. The amplifier MMIC achieves 15.4 dB of gain, 28.3 dBm of IP3, and a P_{sat} of 16.2 dBm at 44 GHz. The corresponding output-stage IP3/P_{dc} ratio is 5.3 which is the best reported for InP-HBTs at Q-band. The MMIC is a high complexity chip which integrates 15 HBTs and 18 Lange couplers in a 6.2x3.5 mm^2 area, and is self-biased through 5V while consuming 108 mA. The "current re-use" enables easier system integration while the "double-balanced" design produces wideband IP3, gain and return-loss performance. This work demonstrates the promising linearity performance of InP-HBTs and its practical biasing capability which is attractive for Q-band receiver applications such as mm-wave digital radio.

Introduction

High IP3 amplifiers are needed in mm-wave receiver systems such as Ka- and Q-band digital radio applications. For frequencies below 18 GHz, GaAs HBTs [1] as well as spiked and pulsed -doped MESFETs [2],[3] have demonstrated record circuit Linearity Figure of Merits (LFOM=IP3/P_{dc}) which are an order of magnitude better than conventional MESFET amplifiers. However for the mm-wave regime, little has been published on the circuit linearity merits of these technologies. One reason is that there are more considerations at these frequencies such as gain or # of gain stages, bandwidth performance, and practical bias implementation. At mm-wave frequencies HBT technology can provide practical monolithic self-bias as well as high IP3 performance.

Recently a GaAs/AlGaAs HBT amplifier was reported which achieved an IP3 of 24-30 dBm and an LFOM of 3-11.6 in a band from 38-44 GHz [4]. An InP-HBT amplifier has also been reported which achieved an IP3 of 26.5 dBm and an LFOM of 4.1 at 35 GHz [5]. InP-HBTs can ultimately provide higher gain and frequency performance per unit dc current and power consumption than GaAs-HBTs due to their higher current density and low voltage (bandgap) operation. Furthermore, their lower V_{ce} operation is better suited for "current re-use" biasing techniques. In this work, we report the first amplifier IP3 results of an InP HBT double-balanced amplifier with "current re-use" biasing which achieves IP3's of 25-28.8 dBm from 34-48 GHz. The output-stage linearity figure of merit (LFOM) is 5.3 at 44 GHz and is the highest reported for InP-HBTs at this frequency.

InAlAs/InGaAs-InP HBT Device Technology

The MMICs reported in this work are based on InAlAs/InGaAs-InP HBT device technology. Fig. 1 shows a cross section of TRW's InAlAs/InGaAs HBT device structure. The InAlAs/InGaAs HBT device epitaxy structure is grown by molecular beam epitaxy (MBE) on a semi-insulating 3-inch InP substrate. Be and Si are used as p- and n-type dopants for the base and emitter/collector, respectively. The emitter incorporates a 750Å InGaAs cap which is highly doped to obtain low emitter contact resistance. The intrinsic emitter region is 1900Å thick and doped to $5x10^{17}$ cm^{-3}. The base-emitter junction is compositionally graded from InGaAs to InAlAs to form HBTs with very repeatable beta and low V_{be} characteristics. The base-collector epitaxial structure consists of a base thickness of 800Å uniformly doped to $3x10^{19}$ cm^{-3}, a 7000Å thick n-type collector lightly doped to $1x10^{16}$ cm^{-3}, and an N+ sub-collector doped to $5x10^{18}$ cm^{-3}. The HBT dc beta across the wafers are typically > 25 at a current density of J_c=40 kA/cm^2. The breakdown voltage BV_{ceo} is 8V and the BV_{cbo} is 13 V which is more than adequate for most RF applications.

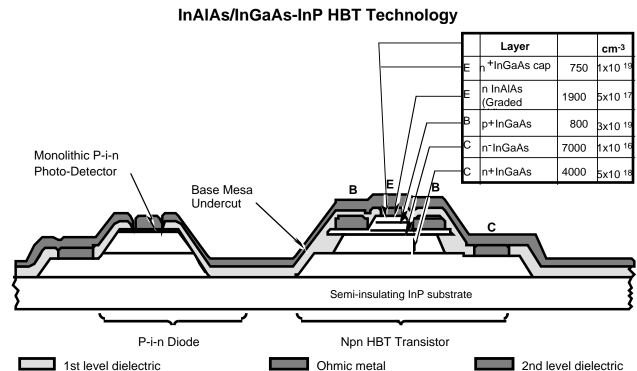

Fig. 1 A cross section of the InAlAs/InGaAs HBT device structure.

A fully self-aligned HBT process is used to produce 1 µm emitter-width HBTs. The HBTs also feature a base-mesa undercut profile that enables a 30-40%

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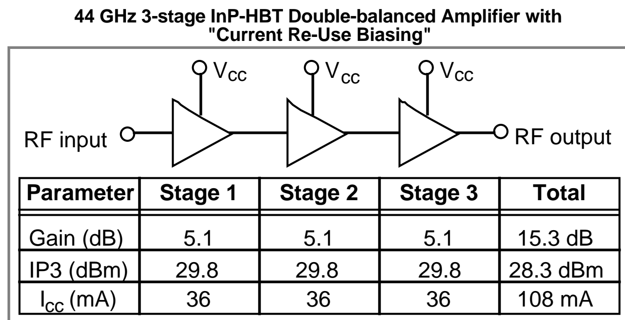
reduction in C_{cb} capacitance, and results in improved device f_T and f_{max}, as well as mm-wave circuit performance [6],[7]. The 1-μm emitter width base-undercut HBTs used in the amplifier design of this work have peak f_T's and f_{max}'s of 80 GHz and 200 GHz (from unilateral gain), respectively. These numbers were achieved from a 1x10 μm^2 quad-emitter HBT biased at a current density of J_C 50-60 kA/cm^2 and a V_{ce}= 2.0V. The high f_{max} and low V_{ce} operation of these InP HBTs make them well suited for the 44 GHz high linearity current share amplifier topology of this work.

High Intercept Amplifier Design

Fig. 2 shows a block diagram and gain-IP3 budget of the 3-stage 44 GHz InP HBT amplifier. A three stage amplifier design is needed to obtain a practical gain of 15.3 dB at 44 GHz. Because of the low gain per stage of 5.1 dB, the first two stages must have a relatively high IP3 with respect to the output stage in order to minimize IP3 degradation through the amplifier chain in accordance with the cascaded IP3 equations. In this design the 1st and 2nd stages are identical to the high IP3 output stage in order to obtain a cumulative IP3 of 28.3 dBm. The overall IP3 is only degraded by 1.5 dB by cascading the three stages. It should be noted that cascode stages were considered for obtaining more gain per stage, however, simulations indicate that this configuration is detrimental to IP3 and also would have precluded the use of the "current share" bias approach in a fixed 5V system.

44 GHz 3-stage InP-HBT Double-balanced Amplifier with "Current Re-Use Biasing"



Parameter	Stage 1	Stage 2	Stage 3	Total
Gain (dB)	5.1	5.1	5.1	15.3 dB
IP3 (dBm)	29.8	29.8	29.8	28.3 dBm
I_{CC} (mA)	36	36	36	108 mA

Fig. 2 Block diagram and gain-IP3 budget of the 3-stage 44 GHz InP-HBT amplifier.

Fig. 3 shows a detailed schematic of the single-stage "double balanced" amplifier with "current re-use". Bias current is shared between adjacent pre-matched 1x10μm^2 x four-emitter-finger (1x10QEC) HBT transistor cells. This reduces the overall amplifier current consumption by 40% for a standard 5V supply. The current sharing between adjacent matched transistor cells is done by a totem pole connection where the emitter of the top cell is fed to the collector of the bottom cell. A bypass capacitor on the emitter of the top cell is used to provide an RF-ground for common-emitter operation. It should be noted that the value of this capacitor must be chosen very carefully in order to maintain the stability performance of the amplifier. A series damping resistor was found to help the stability performance in the simulations, but was not required. A V_{cc} potential of 5V was equally split across the top and bottom 1x10QEC HBT pre-matched cells which have V_{ce}'s of 2.5V each. The current share is well suited with the single stage "double-balanced" amplifier topology which integrates the four pre-matched HBT cells using 6 Lange couplers. The Lange coupler balanced design enables high IP3-bandwidth performance with excellent return-loss.

Single-stage Double Balanced Amplifier with Consolidated current bias

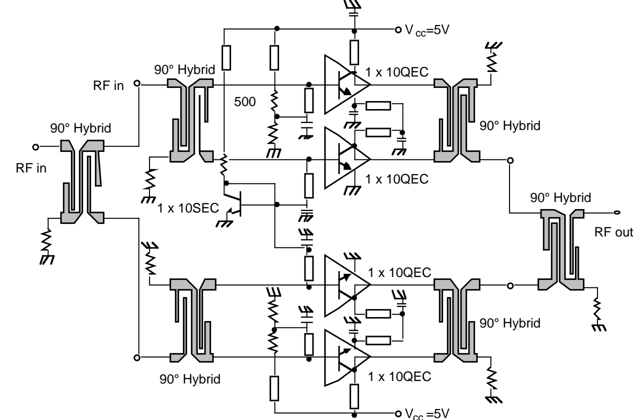


Fig. 3 Detailed schematic of the single-stage "double balanced" amplifier with "current re-use".

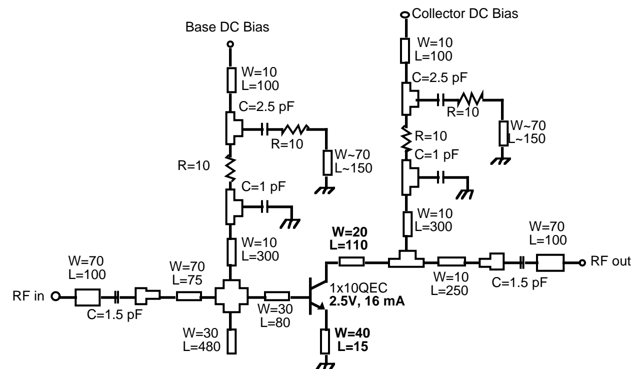


Fig. 4 Detailed schematic of the pre-matched 1x10μm^2 x 4-finger HBT cell

Fig. 4 shows the detailed schematic of the pre-matched 1x10μm^2 x 4-finger HBT cell (1x10QEC) which is biased to an I_{ce}= 16 mA and a V_{ce}= 2.5V. The topology consists of simple series-shunt microstrip matching networks for the input and output which is centered at 44 GHz. Harmonic balance based on a previously reported HBT IP3 model [8] was used to tune for IP3 at 44 GHz. The model was fit to scattering parameters and IP3 data for both HBT device and matched amplifier test structures across a broad frequency range. Fig. 5 gives the simulated single-ended matched 1x10μm^2 x4-finger HBT cell IP3, IP2, gain and optimum output load match using the model. IP3 load-pull simulations were useful in obtaining a 3 dB improvement

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in IP3 performance over the conventional gain matching approach.

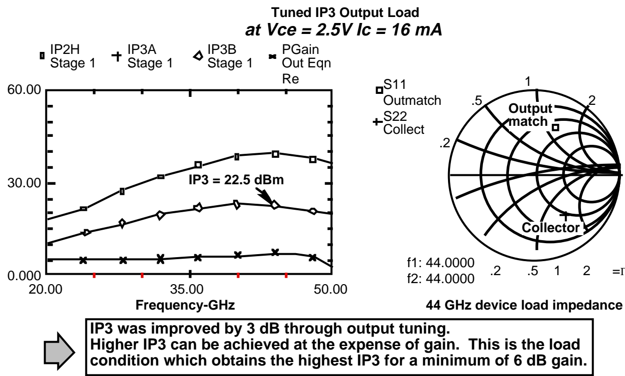

Fig. 5 Simulated pre-matched 1x10μm^2 x4-finger HBT cell IP3, IP2, gain and optimum output load match.

Fig. 6 shows a microphotograph of the 3-stage double-balanced amplifier MMIC. The InP HBT MMIC chip is 6.2x3.5 mm^2 in area and integrates 15 HBTs and 18 Lange couplers and is fully self-biased through a 5V supply.

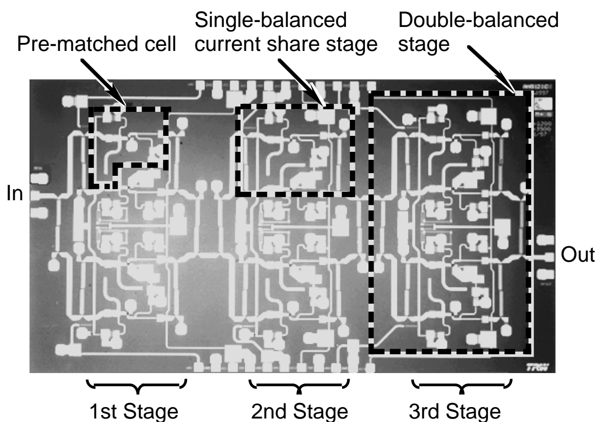

Fig. 6 Microphotograph of the 3-stage "double-balanced" InP-HBT amplifier with "current re-use". Chip area=6.2x3.5 mm^2.

Measured Results

Fig. 7 gives the measured gain and return-loss performance. The simulated gain is also shown for comparison. A gain of 15.4 dB is achieved at 44 GHz with input and output return-losses better than -15 dB across a 25-50 GHz band. The excellent return-loss is due to the use of the balanced Lange coupler amplifier topology. The simulated gain matches the data to within 1 dB at 44 GHz, however, the simulation is more optimistic at lower frequencies. This is believed to be due to the proximity effects of the layout which was not simulated using electro-magnetic simulation tools.

Fig. 8 gives the measured versus simulated IP3 under the nominal design bias. The measured IP3's are 28.3 and 28.8 dBm at 44 and 46 GHz, respectively. At 44 GHz, the calculated IP3/P_{dc} linearity figure-of-merit for the output stage is 5.3:1 and is believed to be the highest reported for an InP-based HBT amplifier in the 44 GHz frequency regime. This number is calculated from the single stage IP3 of 29.8 dBm which is the extracted output stage IP3 given in the gain-IP3 chain analysis of Fig. 2. Note that the IP3 matches reasonable well across a 35-48 GHz band with the exception of a dip in the measured IP3 at around 40 GHz. This correlates to a dip in the gain response which was also evident in the scattering parameter measurements. This dip is believed to be caused by internal RF coupling between the current shared pre-matched stages, however, this discrepancy occurs in a region outside of the 44 GHz band of interest. Fig. 9 also gives the measured IP3 and gain at low, medium and high bias current. It is shown that as the current is increased from 81 mA to 135 mA through the MMIC, the gain improves by as much as 5 dB. However IP3 appears to be optimal at the nominal design current of 108 mA and is probably due to the optimal IP3 matching conditions at this bias level. Fig. 10 is a plot of the output characteristics. The saturated output power, P_{sat}, of this amplifier is 16.2 dBm.

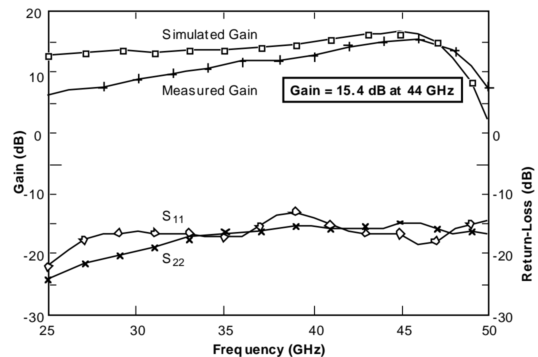

Fig. 7 Measured gain and return-loss performance vs. simulated gain.

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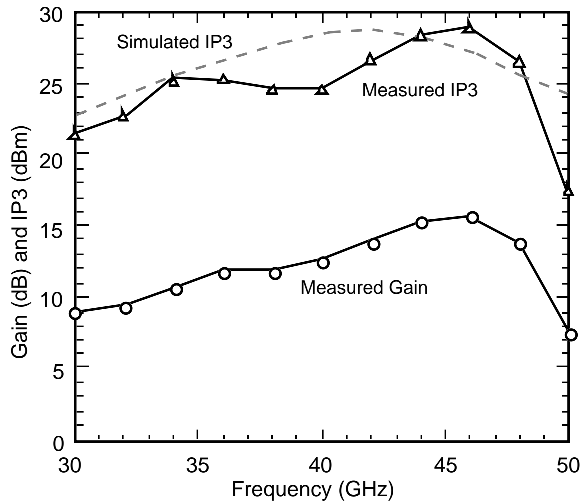

Fig. 8 Measured vs. simulated IP3 at the nominal design bias (5V, 108 mA).

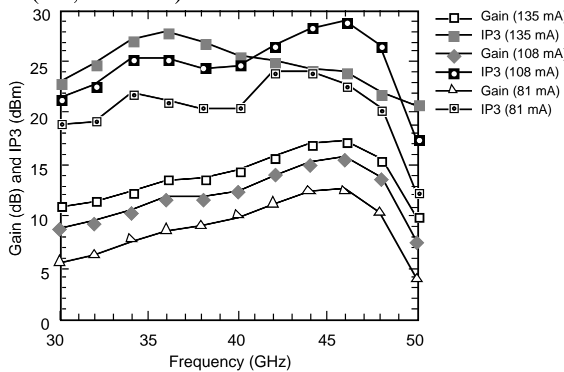

Fig. 9 Measured IP3 and gain at low, medium and high current bias

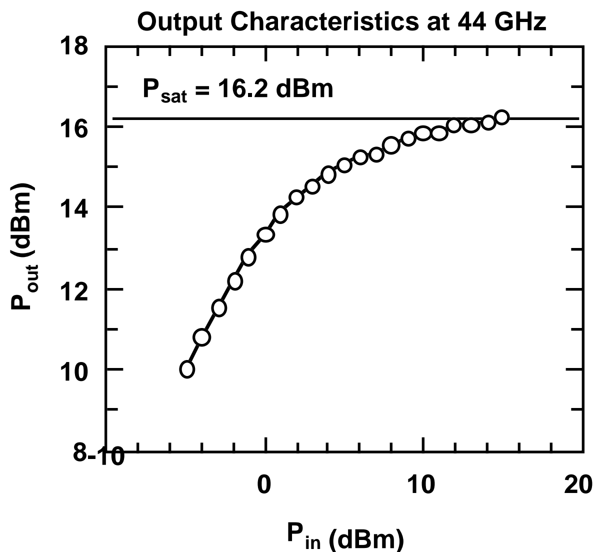

Fig. 10 Measured output power characteristics at 44 GHz

Conclusion

The high IP3 performance and practical bias feasibility of an InP-HBT based 44 GHz amplifier was demonstrated. A single stage IP3/P_{dc} ratio of 5.3:1 was achieved at 44 GHz and is believed to be the highest reported for an InP HBT amplifier at this frequency. An HBT IP3 model and load-pull simulations were used in designing a 3 dB improvement in IP3 of the pre-matched cell. In addition, a practical current share bias approach was employed with the double-balanced HBT amplifier design topology which resulted in a 40% reduction in current consumption through a standard 5V supply. The high IP3, mm-wave frequency and low voltage performance of InP HBTs make them attractive for commercial digital radio receiver applications.

Acknowledgment

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References

[1] B.L Nelson, D.K. Umemoto, C.B. Perry, R. Dixit, B.R. Allen, M.E. Kim, and A.K. Oki, "High-linearity, Low DC Power Monolithic GaAs HBT Broadband Amplifiers to 11 GHz," 1990 IEEE MMWMC-S Dig., Dallas, TX, pp. 15-18.

[2] S.L.G. Chu, J.C. Huang, A. Bertrand, M.J. Schindler, W. Struble, R. Binder, W. Hoke, "High Linearity Monolithic Broadband Pseudomorphic Spike-Doped MESFET Amplifiers," 1992 IEEE GaAs IC Symp. Dig., pp. 211-214.

[3] P.K. Ikalainen, L.C. Witkowski, and K.R. Varian, "Low Noise, Low dc Power Linear Amplifiers," 1993 IEEE MMWMC-SDig., Atlanta, GA, pp. 159-162.

[4] Y. Kwon, W.-J. Ho, J.A. Higgins, "A Q-Band Monolithic Linear Amplifier Using AlGaAs/GaAs HBT's," IEEE MGWL, vol. 6, no. 4, April 1996, pp. 180-182.

[5] K.W. Kobayashi, A.K. Oki, J. Cowles, L.T. Tran, P.C. Grossman, T.R. Block, and D.C. Streit, "The Voltage-Dependent IP3 Performance of a 35-GHz InAlAs/InGaAs-InP HBT Amplifier," IEEE MGWL, vol. 7, no. 3, March 1997, pp. 66-68.

[6] K.W. Kobayashi, L.T. Tran, J. Cowles, T.R. Block, A.K. Oki, and D.C. Streit, "Low dc power High

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

Gain-Bandwidth Product InAlAs/InGaAs-InP HBT Direct-Coupled Amplifiers," IEEE GaAs IC Symposium Dig., Orlando, FL, 1996, pp. 141-144.

[7] K.W. Kobayashi, J. Cowles, L.T. Tran, T.R. Block, A.K. Oki, and D.C. Streit, "A 2-50 GHz InAlAs/InGaAs-InP HBT Distributed Amplifier," IEEE GaAs IC Symposium Dig., Orlando, FL, 1996, pp. 207-210.

[8] S.A. Maas, B.L. Nelson, D.L. Tait, "Intermodulation in Heterojunction Bipolar Transistors," IEEE trans. on MTT, vol. 40 no. 3, march 1992, pp. 442-448.

0-7803-4471-5/98/$10.00 (c) 1998 IEEE